Listing of Claims:

Please amend claim 1, cancel claims 8 and 9 without prejudice or disclaimer, and add new claims 21-27 as indicated in the following listing of claims, which replaces all prior versions.

1. (Currently amended) A down converter, comprising:

an integrated circuit having a control Field Effect Transistor (FET) (CF) disposed in a first well having a first polarity and a synchronous rectifier FET (SF) disposed in a second well having a second polarity opposite the first polarity, wherein the control FET is a Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS), and a conductivity-type of the LDMOS FET and a conductivity-type of a substrate are of the same type.

2. (Previously presented) A down converter as recited in claim 1, wherein the synchronous rectifier FET is a Vertical Double-Diffused Metal Oxide Semiconductor (VDMOS) FET.

3. (Original) A down converter as recited in claim 1, wherein the synchronous rectifier FET is a vertical trench DMOS FET.

4. (Withdrawn) A down converter as recited in claim 1, wherein the synchronous rectifier FET is another Lateral Double-Diffused Metal Oxide Semiconductor (LDMOS) FET.

5. (Withdrawn) A down converter as recited in claim 2, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET to an output on a surface of a substrate.

6. (Withdrawn) A down converter as recited in claim 3, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic

connection of a few milli-Ohms from a source of the control FET to an output on a surface of a substrate.

7. (Withdrawn) A down converter as recited in claim 4, further comprising a plurality of conductive plugs connected electrically in parallel, which provide an ohmic connection of a few milli-Ohms from a source of the control FET and a drain of the synchronous rectifier FET to an output on a surface of a substrate.

8. (Cancelled) A down converter as recited in claim 2, wherein the VDMOS FET and the LDMOS FET are disposed in respective wells having opposite polarity.

9. (Cancelled) A down converter as recited in claim 3, wherein the vertical trench DMOS FET and the LDMOS FET are disposed in respective wells having opposite polarity.

10. (Original) A down converter as recited in claim 1, wherein the integrated circuit does not include isolation regions between the CF and the SF.

11. (Original) A down converter as recited in claim 1, wherein the conductivity type is n-type.

12. (Withdrawn) A down converter, comprising an integrated circuit having a control FET (CF) and a synchronous rectifier FET (SF), wherein the control FET and the synchronous rectifier FET are each LDMOS FETs, and a conductivity-type of the LDMOS FETs and a conductivity of the substrate are of the same conductivity type.

13-20. (Cancelled).

21. (New) A down converter as recited in claim 1, wherein the integrated circuit further includes one or more additional FETs configured to control gate switching of the control FET and the synchronous rectifier FET.

22. (New) A down converter as recited in claim 1 further comprising an inductor, wherein a source contact of the control FET and a drain contact of the synchronous rectifier FET are connected to the inductor of the down converter.

23. (New) A down converter as recited in claim 1 further comprising an inductor, wherein a source contact of the control FET and a drain contact of the synchronous rectifier FET are connected to the inductor of the down converter, the source contact of the control FET and the drain contact of the synchronous rectifier FET further having low-ohmic connections to mitigate resistive and inductive parasitics of the integrated circuit.

24. (New) A down converter as recited in claim 23, wherein the integrated circuit has a parasitic inductance on the order of 1 nH or less.

25. (New) A down converter as recited in claim 1 further including a voltage input, wherein the control FET has a drain contact connected to the voltage input of the down converter and the control FET has a source contact connected to a drain contact of the synchronous rectifier FET.

26. (New) A down converter as recited in claim 25, wherein the source contact of the control FET is connected to the drain contact of the synchronous rectifier FET via a conductive plug in the substrate.

27. (New) A down converter as recited in claim 1 wherein the control FET includes a gate driven by a control block supplied by an external capacitor.